IN THE CLAIMS

Please amend claim 44 as follows:

1-17. (Canceled)

18. (Previously Presented) A semiconductor chip comprising:

a passive first region on a top side of the semiconductor chip;

an active second region on the top side of the semiconductor chip;

an arrangement of contact areas and test areas having respective top surfaces which are arranged in a common plane, the contact areas and test areas are in each case electrically conductively connected to one another via a conduction web that has a top surface that lies in the common plane, the contact areas being arranged in the passive first region, the passive first region having no active components of an integrated circuit, the test areas being arranged in the active second region, the active second region having active components of an integrated circuit, and wherein the test areas are sealed and the contact areas are not sealed;

an insulating layer situated between the top side and a lower plane;

through contacts extending through a portion of the insulating layer directly below the conduction web and extending from the conduction web to the lower plane, the through contacts being connected to interconnects that are connected to electrodes of the components of the integrated circuit;

wherein portions of the insulating layer directly below the contact areas and the test areas are free from the through contacts.

19. (Previously Presented) The semiconductor chip of claim 18, comprising wherein the insulating layer includes silicon dioxide and/or silicon nitride arranged between the components of an integrated circuit and the test areas of the semiconductor chip.

20-21. (Cancelled)

22. (Previously Presented) The semiconductor chip of claim 18, comprising wherein the interconnects to the electrodes of the components of the integrated circuit comprise copper or a copper alloy.

23. (Previously Presented) The semiconductor chip of claim 18, comprising wherein the contact areas and the test areas at their edges and the conduction web on its top side have a multilayer insulation and passivation layer.

24. (Previously Presented) The semiconductor chip of claim 23, comprising wherein the multilayer insulation and passivation layer includes a silicon dioxide layer arranged directly on the edges of the contact areas and of the test areas and on the connecting conduction web.

25. (Previously Presented) The semiconductor chip of claim 23, comprising wherein the multilayer insulation and passivation layer comprises a silicon nitride layer and a polyimide layer.

26. (Previously Presented) The semiconductor chip of claim 18, comprising wherein the conduction web is formed in T having a transverse bar and a longitudinal bar, the transverse bar of the T having a width about equal to a width of the contact areas and having through contacts to interconnects, while the longitudinal bar of the T has a width determined in response to the maximum current loading during testing by test tips.

27. (Previously Presented) The semiconductor chip of claim 18, comprising wherein the test areas have a width (b_P) about equal to a width of the contact areas and have a length (l_P) greater than their width (b_P).

28. (Previously Presented) An electronic device comprising:

a semiconductor chip, the semiconductor chip having an arrangement of contact areas and test areas which are arranged in a common plane and are in each case electrically conductively connected to one another via a conduction web that lies in the common plane, the contact areas being arranged in a passive, first region of a top side of the semiconductor chip, the passive first region having no active components of an integrated circuit, wherein the test areas are sealed and the contact areas are not sealed;

the test areas being arranged in an active, second region of the top side of the semiconductor chip, the active second region having active components of an integrated circuit;

the test areas and contact areas being formed in the same interconnect plane;

the length (lp) of the test areas being at least approximately 1.5 times greater than the width (bp) thereof;

an insulating layer situated between the top side and a lower plane;

through contacts extending through a portion of the insulating layer directly below the conduction web and extending from the conduction web to the lower plane, the through contacts being connected to interconnects that are connected to electrodes of the components of the integrated circuit;

wherein portions of the insulating layer directly below the contact areas and the test areas are free from the through contacts.

29. (Previously Presented) The electronic device of claim 28, the semiconductor chip wherein:

the insulating layer includes silicon dioxide and/or silicon nitride arranged between the components of an integrated circuit and the test areas of the semiconductor chip.

30. (Previously Presented) The electronic device of claim 29, comprising wherein the interconnects to the electrodes of the components of the integrated circuit comprise copper or a

copper alloy.

31. (Previously Presented) The electronic device of claim 30, comprising wherein the contact areas and the test areas at their edges and the conduction web on its top side have a multilayer insulation and passivation layer, and wherein the multilayer insulation and passivation layer includes a silicon dioxide layer arranged directly on the edges of the contact areas and of the test areas and on the connecting conduction web.

32. (Previously Presented) The electronic device of claim 30, comprising wherein the multilayer insulation and passivation layer comprises a silicon nitride layer and a polyimide layer.

33. (Previously Presented) The semiconductor chip of claim 29, comprising wherein the conduction web is formed in T having a transverse bar and a longitudinal bar, the transverse bar of the T having a width about equal to a width of the contact areas and having through contacts to interconnects, while the longitudinal bar of the T has a width determined in response to the maximum current loading during testing by test tips.

34. (Withdrawn) A method for post processing of a semiconductor wafer comprising:

providing the semiconductor wafer comprising a plurality of semiconductor chips having a passive first region and an active second region, the semiconductor chips having an arrangement of contact areas and test areas which are electrically conductively connected to one another, the contact areas being arranged in the passive first region of the top side of the semiconductor chip, the passive first region having no components of an integrated circuit, and the test areas being arranged in the active second region of the top side of the semiconductor chip, the active second region having components of an integrated circuit;

carrying out a functional test with a test device having test tips to determine defective semiconductor chips;

marking the defective semiconductor chips.

35. (Withdrawn) The method of claim 34, ccomprising sealing of the test areas.

36. (Withdrawn) The method of claim 35, comprising sealing the test areas by application of a patterned photoresist layer or soldering resist layer.

37. (Withdrawn) The method as claimed in one of claims 34, comprising arranging the test tips in offset fashion from test area to test area when carrying out a functional test.

38. (Previously Presented) A semiconductor wafer comprising:

a plurality of semiconductor chips having a passive first region and an active second region, the semiconductor chips having an arrangement of contact areas and test areas which are arranged in a common plane and are electrically conductively connected to one another via a conduction web that lies in the common plane, wherein the test areas are sealed and the contact areas are not sealed;

the contact areas being arranged in the passive first region of the top side of the semiconductor chip, the passive first region having no active components of an integrated circuit; and

the test areas being arranged in the active second region of the top side of the semiconductor chip, the active second region having active components of an integrated circuit;

an insulating layer having through contacts arranged in the region of the conduction web and extending from the conduction web to a lower plane, the through contacts being connected to interconnects that are connected to electrodes of the components of the integrated circuit;

wherein the contact areas and the test areas are free from the through contacts;

each of the semiconductor chips being defined by a boundary extending around the respective semiconductor chip, the contact areas and the test areas are completely situated within the boundary the respective semiconductor chip.

39. (Previously Presented) A semiconductor chip comprising:

a passive first region on a side of the semiconductor chip;

an active second region on the side of the semiconductor chip;

an arrangement of contact areas and test areas which are arranged in a common plane and are in each case electrically conductively connected to one another via a conduction web that lies in the common plane, the contact areas being arranged in the passive first region, the passive first region having no active components of an integrated circuit, the test areas being arranged in the active second region, the active second region having active components of an integrated circuit, wherein the test areas are sealed and the contact areas are not sealed; and

an insulating layer situated between the top side and a lower plane ;

through contacts extending through a portion of the insulating layer directly below the conduction web and extending from the conduction web to the lower plane, the through contacts being connected to interconnects that are connected to electrodes of the components of the integrated circuit;

wherein portions of the insulating layer directly below the contact areas and the test areas are free from the through contacts.

40. (Cancelled).

41. (Previously Presented) The semiconductor chip of claim 18, wherein each of the contact areas is electrically conductively connected to a respective one of the test areas by the conduction web extending between and in the same plane as the contact area and the respective test area.

42. (Previously Presented) The semiconductor chip of claim 18, further comprising:

a boundary defining the area of the semiconductor chip;

a continuous metalized area situated within the boundary;

wherein the contact areas and the test areas are formed on the metalized area, such that the contact areas and the test areas are situated within the boundary the semiconductor chip.

43. (Previously Presented) The semiconductor chip of claim 18, wherein the test areas are sealed with a patterned photoresist layer.

44. (Currently Amended) The semiconductor chip of claim 18, wherein the ~~contact~~ test areas are sealed with a soldering resist layer.